REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested. Applicants observe that Claims 1-13 are pending in this application and that no previous amendments to the claims were made.

Original Claims 1, 3, 4, 5, 6, 9, 10 and 12 were objected to because of various informalities mentioned under item 2 of the outstanding Office Action. In response to the informal objection to the aforementioned claims, applicants have amended Claims 1, 3, 4, 5, 6, 9, 10 and 12 in the manner proposed by the Examiner in the present Office Action. In view of the above amendments to the claims, applicants submit that the informal objection to the claims can and should be withdrawn. Reconsideration and withdrawal of the claim objection are thus respectfully requested.

Claims 1, 2 and 9-13 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of U.S. Patent No. 6,472,919 to Burr et al. ("the '919 patent") and U.S. Patent No. 4,542,485 to Iwahashi et al.("Iwahashi et al."). Claims 3-8 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of the '919 patent, Iwahashi et al., and U.S. Patent No. 5,622,880 to Burr et al. ("the '880 patent").

Applicants respectfully submit that the claimed method of the present application is not rendered obvious from the combined disclosures of the '919 patent, Iwahashi et al., and optionally the '880 patent since the applied references do not teach or suggest the claimed processing steps that are recited in Claim 1 of the present application. Specifically, the applied references do not teach or suggest the claimed method for compensating threshold voltage roll-off within a semiconductor chip or system which

includes designing a semiconductor chip or system having a plurality of transistor devices in which channel length of each transistor device is equal to L_{nom}; *setting off-current of each transistor device to I-off$_{max}$ by predetermining that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor device such that its threshold voltage is equal to Vt_{min}; testing off-current of each transistor device*; and biasing the back gate or body nodes of some transistor devices, each of which has an off-current that does not meet a preselected specification of about I-off$_{max}$, to increase threshold voltage of each of said transistor devices to about Vt_{min} thereof thereby compensating the threshold voltage roll-off within said semiconductor chip or system.

The '919 patent provides low voltages latches that, in accordance with one embodiment, each have the same channel length and channel width. Applicants note that in accordance with the '919 patent such low voltages latches having equal channel dimensions are critical in maintaining a constant threshold voltage. The '919 patent does not teach or suggest the claimed method for compensating for the threshold voltage roll-off effect by *setting off-current of each transistor device to I-off$_{max}$ by predetermining that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor device such that its threshold voltage is equal to Vt_{min}; testing off-current of each transistor device; and biasing the back gate or body nodes of some transistor devices, each of which has an off-current that does not meet a preselected specification of about I-off$_{max}$, to increase threshold voltage of each of said transistor devices to about Vt_{min} thereof thereby compensating the threshold voltage roll-*

off within said semiconductor chip or system. The aforementioned processing steps of the present invention are not taught or suggested in the '919 patent.

Iwahashi et al. do not alleviate the above mentioned defect in the '919 patent since the applied secondary reference also does not teach or suggest a method for compensating for threshold voltage roll-off by *setting off-current of each transistor device to I-off$_{max}$ by predetermining that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor device such that its threshold voltage is equal to Vt_{min}; testing off-current of each transistor device*; and biasing the back gate or body nodes of some transistor devices, each of which has an off-current that does not meet a preselected specification of about I-off$_{max}$, to increase threshold voltage of each of said transistor devices to about Vt_{min} thereof thereby compensating the threshold voltage roll-off within said semiconductor chip or system.

Iwahashi et al. do disclose that a back gate bias can be applied to compensate for a decrease in threshold voltage; however, the applied reference does not teach or suggest utilizing the same in combination with applicants' other claimed processing steps. In particularly, using the back gate biasing with the step of *setting off-current of each transistor device to I-off$_{max}$ by predetermining that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor device such that its threshold voltage is equal to Vt_{min}.*

As such, the combination of the '919 patent and Iwahashi et al. does not render the claimed method obvious.

With respect to the tertiary applied reference, i.e., the '880 patent, that applied reference does not alleviate the above mentioned defects in the combination of the '919

patent and Iwahashi et al. since the '880 patent also does not teach or suggest the claimed method for compensating for threshold voltage roll-off by utilize steps which include, among others, *setting off-current of each transistor device to I-off$_{max}$ by predetermining that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor device such that its threshold voltage is equal to Vt_{min}; testing off-current of each transistor device*; and biasing the back gate or body nodes of some transistor devices, each of which has an off-current that does not meet a preselected specification of about I-off$_{max}$, to increase threshold voltage of each of said transistor devices to about Vt_{min} thereof thereby compensating the threshold voltage roll-off within said semiconductor chip or system.

The '880 patent does disclose that the threshold voltage can be controlled by dopant implantation; however, such teaching does not make obvious the claimed step of *setting off-current of each transistor device to I-off$_{max}$ by predetermining that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor device such that its threshold voltage is equal to Vt_{min}.*

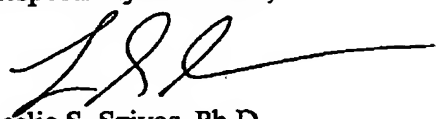
As such, the combination of the '919 patent, Iwahashi et al. and the '880 patent does not render the claimed method obvious.

The various §103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed methods to include the various steps recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the

desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested. Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



Leslie S. Szivos, Ph.D.
Registration No. 39,394

SCULLY, SCOTT, MURPHY & PRESSER, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343
Customer No. 23389
LSS:vh